

Compact MMIC active inductor

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Abstract — An active inductor implementation suitable for microwave and millimeter wave applications is introduced. The circuit is very simple, compact and can be easily realized in a floating configuration. Simulations, based on Philips smart library ED02AH, show that the component can have a quality factor in excess of 100 at 22 GHz with a current consumption of 5.5 mA @ 2.5V bias. A monolithic implementation in PHEMT technology is reported and discussed.

I. INTRODUCTION

The implementation of high Q active inductor at millimeter wave frequencies has been widely investigated [1-9] but it is still a challenging and open problem. The availability of such component is very useful for the implementation of filtering structures, voltage controlled oscillators, inductive peaking techniques and many other applications.

In this work an active inductor topology and implementation, using a single transistor (a PHEMT), is presented, resulting in a very simple and highly integrable component.

The proposed approach to the synthesis problem of the active inductor starts from a well-founded theory as successfully done in [9]. As it will be explained in the following paragraphs, the resulting MMIC implementation is easy to design and fairly scalable in the millimeter wave frequency range.

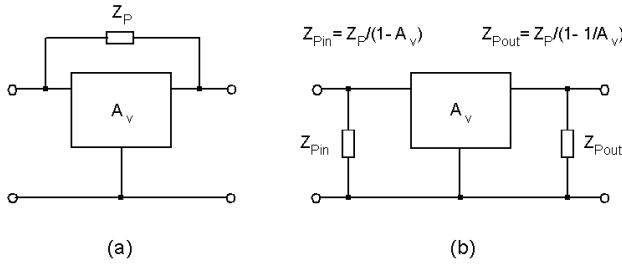


Fig. 1. Miller theorem equivalent circuit.

II. BASIC THEORY

The well known Miller's theorem states that when an impedance, Z_P , is connected between input and output terminals of an amplifier with a voltage gain, A_v , the

circuit is equivalent to the same amplifier with two impedances, Z_{Pin} and Z_{Pout} , in parallel to its input and output terminals as shown in Fig.1, where:

$$Z_{Pin} = \frac{Z_P}{(1-A_v)}$$

$$Z_{Pout} = \frac{Z_P}{1 - \frac{1}{A_v}} \quad (1)$$

Assuming a Common-Source FET as the gain element, its voltage gain can be approximately expressed by:

$$A_v = -\frac{g_m R_0}{1 + j\omega C_T R_0} \quad (2)$$

where R_0 is the total drain to source resistance (the FET output resistance in parallel with that of the active load) and C_T is the total drain-source capacitance.

Let us assume that Z_P is an inductor with a series resistance representing its losses (Fig. 2):

$$Z_P = R + j\omega L. \quad (3)$$

If the following condition is satisfied

$$\omega \cdot C_T R_0 \gg (1 + g_m R_0), \quad (4)$$

the real part of Z_{Pin} can be reduced by increasing the FET transconductance, g_m , while its imaginary part is essentially the reactance of the initial inductor.

This high-Q inductor is actually in parallel to the gate-source capacitance, hence exploiting the inductive behaviour below the resonant frequency:

$$\omega_{RES} = \frac{1}{\sqrt{LC_{gs}}}, \quad (5)$$

where C_{gs} is the gate to source capacitance. In practice the value of this resonant frequency is well above 50 GHz.

Since a negative resistance is actually used to reduce the losses in the active inductor, the transistor g_m and therefore the device size must be carefully selected, in order to achieve the desired losses reduction and, at the same time, to avoid any possible instability.

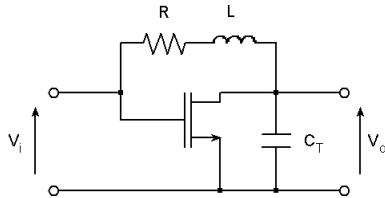


Fig. 2. The Common-Source circuit with Z_p .

For applications at millimeter-wave frequencies the passive inductor can be simply implemented using a narrow transmission line between the input and output terminal, due to the low inductance values usually required in this frequency range.

III. DESIGN PROCEDURE

Once the desired value of inductance, L , is selected, a capacitance must be added in parallel to the drain source capacitance, C_{ds} , that usually results to be too small to guarantee a suitably low operating frequency for the active inductor. Furthermore a larger value of the total capacitance, C_T , will help to choose a suitable value for g_m .

Depending on the values of L, C_T , the losses R and the operating frequency, F , the value of the transistor transconductance, g_m , must be selected in order to maximize the inductor's quality factor, Q :

$$Q = \frac{R \cdot g_m + \omega^2 \cdot L \cdot C_T}{\omega(R \cdot C_T - L \cdot g_m)}. \quad (6)$$

The function above grows for g_m ranging from 0 to the resonant value given by:

$$g_m = \frac{R \cdot C_T}{L}. \quad (7)$$

This value of g_m represents the upper limit of stability for which the losses equal the modulus of the negative resistance produced by T_1 . Thus, in order to maximize the active inductor Q , this condition has to be carefully approached avoiding a neat negative resistance and thus providing a suitable safety margin for circuit stability.

It is worth to note that the critical transconductance value is determined by losses, R , the inductance, L , and the capacitance C_T and can be fairly low, thus allowing for a corresponding extremely low bias current.

These results are analogous to those in [9] and this is perfectly consistent as we are now applying the Miller theorem in its dual form. The advantage in this case is that the inductor can be done floating simply adding a current generator from the source terminal of the amplifier toward ground.

The active inductor performances are affected by the bias circuit. In our case the topology sketched in Fig. 3 has been adopted.

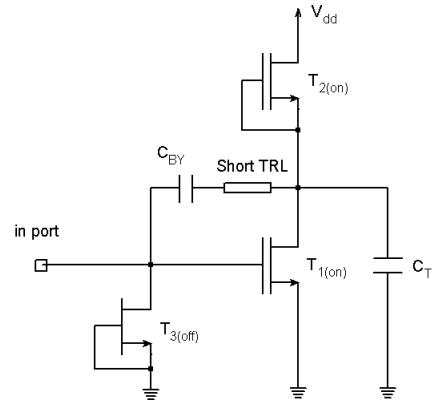


Fig. 3. The active inductor schematic.

The Common-Source FET, T_1 , is actively loaded with an identical transistor, T_2 , with $V_{gs}=0$. T_3 is an enhancement type FET with $V_{gs}=0$. This transistor realize a high resistance path to ground for the gate terminal of T_1 . The connection of the inductance, L , between input and output terminals have to be done through a DC blocking capacitor in order to preserve the bias point of the common source amplifier. The equivalent model of the biased active inductor is reported in Fig. 4, where the shunt resistor and capacitance take into account the loading of the biasing transistor, T_3 , while the series R-L-C circuit models the active inductor according to what previously discussed. The shunt resistor, R_p , is mainly due to the drain to source resistance of T_3 and has values of about $10K\Omega$ while the shunt capacitance is the sum of the gate to source capacitance of T_1 and the drain to source capacitance of T_3 with a total value of about $0.1pF$.

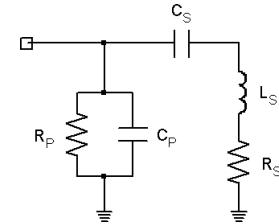


Fig. 4. Active inductor equivalent circuit.

IV. EXPERIMENTS

A prototype inductor has been designed using the Philips ED02AH PHEMT process. As sketched in Fig. 3, the inductor has been implemented with a short transmission line connected to input and output terminals through a bypass capacitor. The capacitor inserted in

parallel to the drain-source capacitance is a MIM capacitor.

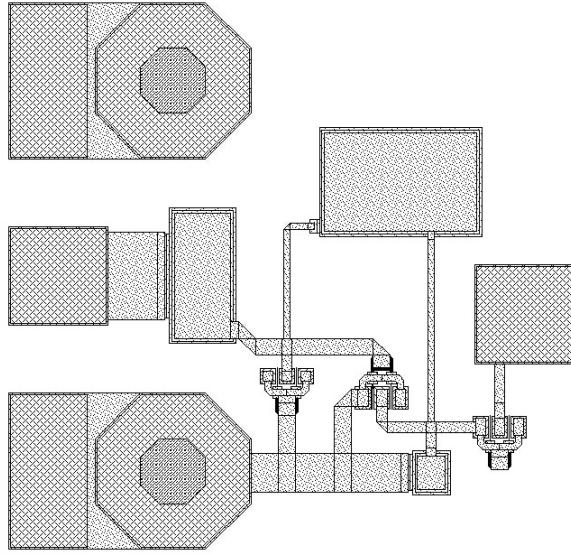


Fig. 5. MMIC layout: dimension $600 \times 600 \mu\text{m}^2$.

The PHEMTs have been modelled using a small-signal equivalent-circuit scalable model to carry out the dimensioning of the active inductor. A large signal SPICE model has been used to evaluate the inductor linearity and distortion.

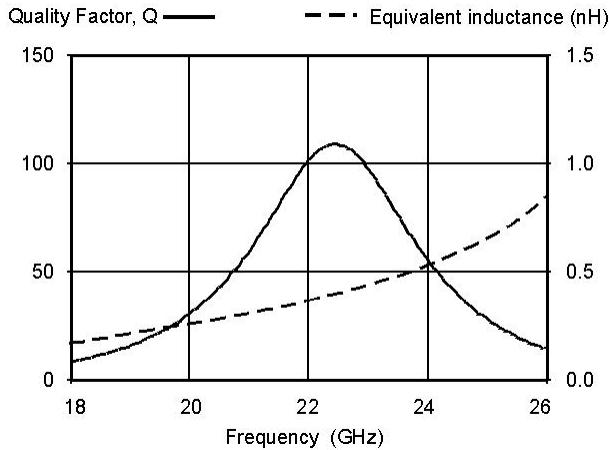


Fig. 6. Active inductor quality factor (left axis) and equivalent inductance in nH (right axis).

The layout of the resulting active inductor is depicted in Fig. 5. The overall chip dimensions are $600 \times 600 \mu\text{m}^2$. It is worth to note that most of the die area is occupied by the coplanar pads ensuring very compact dimensions for the active inductor.

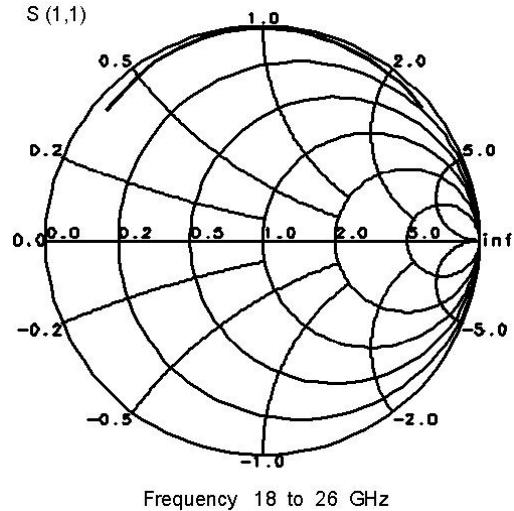


Fig. 7. Active inductor frequency behavior.

In Fig. 6 is reported, on the right axis, the equivalent value of the inductance ($L=0.25\text{nH}$) and, on the left axis, the corresponding Q , that results to be in excess of 100 over a relatively wide frequency range. Making reference to the notation used in Fig. 4, the equivalent inductance is:

$$L_{\text{eq}} = L_s - \frac{1}{\omega^2 C_s}. \quad (8)$$

This inductance has a fairly constant value slowly growing with frequency due to the effect of C_s .

In Fig. 7 is reported the inductance as a function of frequency on the Smith chart.

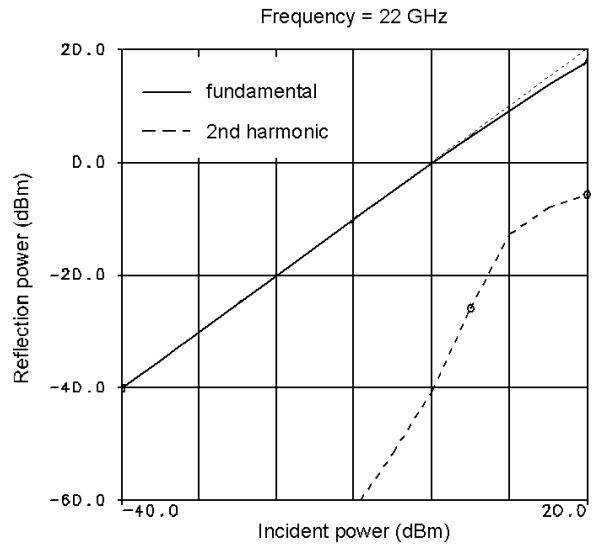


Fig. 8. Active inductor linearity and distortion.

The linearity and distortion of the active inductor was evaluated feeding a fixed frequency 22 GHz signal to the active inductor and measuring the reflected fundamental and second harmonic power components [1]. The input signal was swept in the range $-40 \div +20$ dBm, as reported in Fig. 8. The 1 dB compression point is about 11 dBm with a second harmonic ratio of -20dB.

V. CONCLUSIONS

A novel topology for grounded and floating active inductors has been presented, based on a very simple application of the Miller's theorem. The basic circuit is composed by a single active device loaded by a narrow transmission line. The scheme is featured by extremely reduced and controllable losses, resulting in excellent quality factors, reduced size and low dissipation. A simple implementation of the circuit including bias circuitry has been performed in PHEMT monolithic technology, whose simulation results confirm the proposed approach.

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